EV10AS940-FMC-EVM GUI User Manual

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1 Revision History

Issue	Date	Comments
0.9.0	October 2023	First version for selected customers
0.9.1	December 2023	Version for GUI 1.1.14
0.9.2	December 2023	Version for GUI 1.1.15 and layout
0.9.3	January 2024	Various updates
0.9.4	January 2024	Version for GUI 1.1.16
0.9.5	January 2024	Minor updates
0.9.6	January 2024	First version for GUI 1.2.0
0.9.7	March 2024	First version for GUI 1.2.6
0.9.8	March 2024	First version for GUI 1.2.7

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2 Related Documentation

Table 1: Related Documentation

Document type	Number & Issue	Comments
Preliminary datasheet	DS 60S 221987(B)	https://semiconductors.teledyneimaging.com/en/products/data-converters/ev10as940/
User Guide Hardware		
Digital features description		

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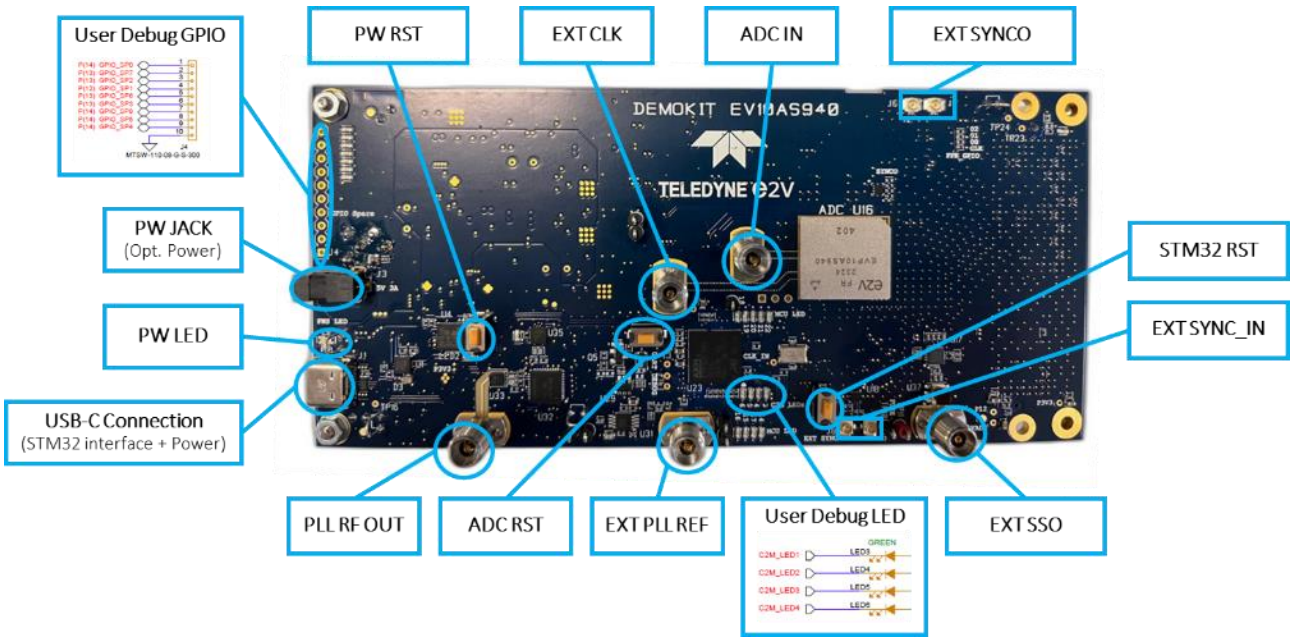
3 Purpose and prerequisites

The goal of this document is to describe the use of the GUI to control the EV10AS940-FMC-EVM:



Additional information on the hardware can be found in the EV10AS940-FMC-EVM user manual.

It is required to first install a few dependencies before starting the GUI:

- NI LabVIEW 2020 SP1 RunTime (LabVIEW Runtime Download - NI)
- NI VISA driver (NI-VISA Download - NI) (NI-VISA and LabVIEW Version Compatibility - NI)
- STM32 microcontroller driver (STSW-STM32102 - STM32 Virtual COM Port Driver - STMicroelectronics)

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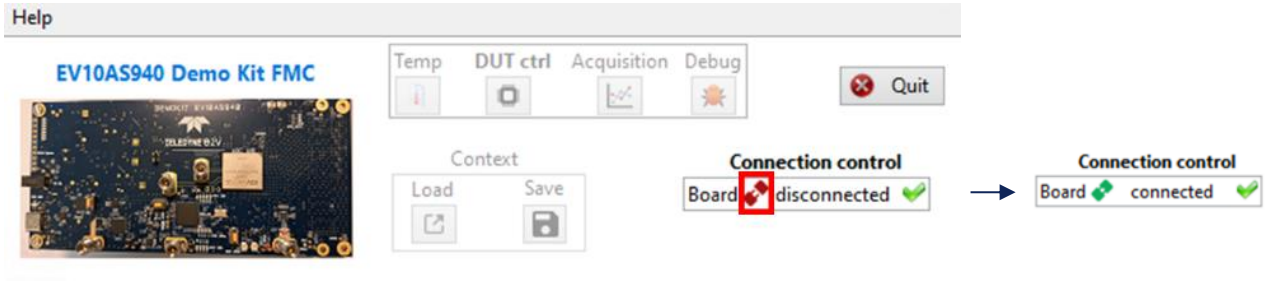
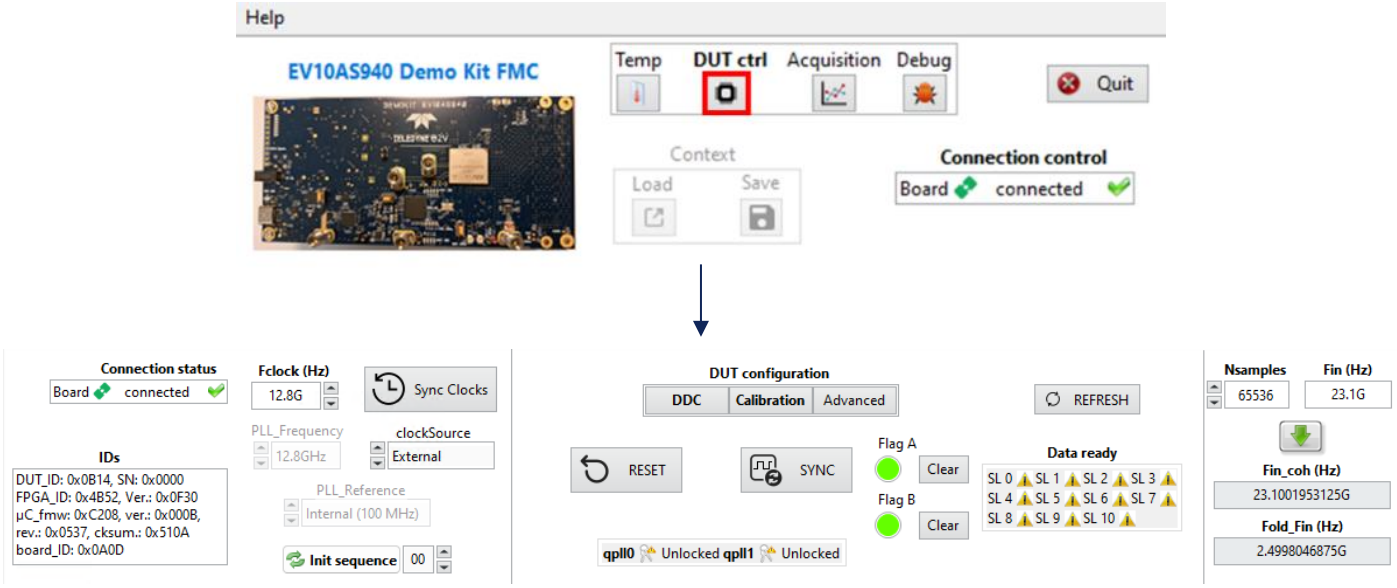
4 Board connection

Once the hardware has been correctly set up and the GUI launched, the main GUI window will be displayed.
The first step is then to establish the connection with the board trough the connect icon displayed below in the red square:



Once the connection is performed, the icon turns green. (If it stays red, check the USB connection to the board and the supply of the board. For additional tests, check the section “Troubleshooting”).

It is now possible to open the DUT control window with the icon highlighted below:



Check whether the DUT, FPGA and µC ID’s visible in the bottom left part are different from 0x0000 to confirm that corresponding registers could be read successfully by SPI.

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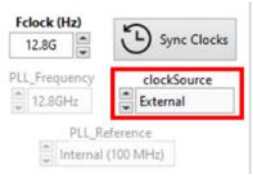
5 Clock configuration

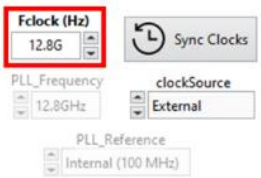
On the left part of the DUT control window, it is possible to configure the clock, that can be either supplied by the on-board PLL (TI LMX2594) or from an external generator:



Current limitation: the board cannot operate for a Fclock frequency in the 7.4 to 7.9 GHz range. This limitation will be removed in a future revision of the software.

5.1 External clock

With the external configuration, it is required to enter the used clock frequency with the “Fclock (Hz)” control:



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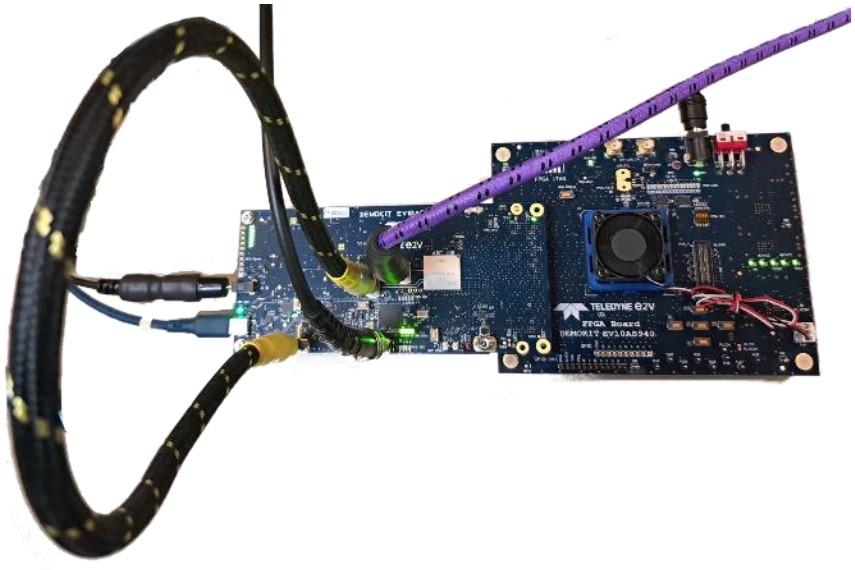
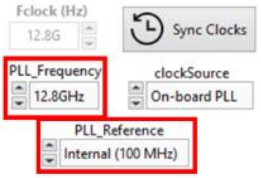
5.2 Internal clock (on board PLL)

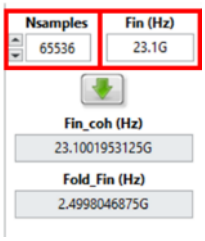


In this configuration, the clock frequency can be selected amongst a list available in the “PLL_Frequency” control. In the GUI folder, a directory contains .txt files used to program the PLL for each available frequency. If other frequencies are required, please contact the Hotline to get new files.
The PLL reference can bet set to internal or external. In this last case, a 10 MHz signal must be supplied and the LED23 should turn on to validate that the external reference has been considered.



5.3 Coherent frequency calculation :

On the right part of the window, a tool can be used to calculate the coherent frequency, computed from a desired input frequency Fin(Hz), the clock frequency and the number of samples required (Nsamples):



The folded coherent frequency in the first Nyquist zone is also displayed (Fold_Fin (Hz)).

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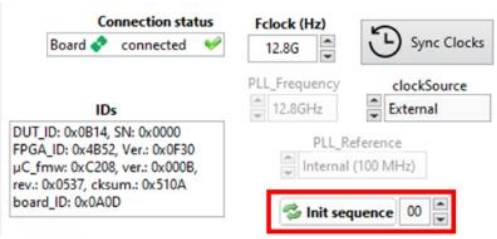
5.4 Synchronize High Speed Serial Links (HSSL)

Once the clock has been configured, the next step is to synchronize the HSSLs used to transfer the data. This procedure is performed via the same DUT control window.

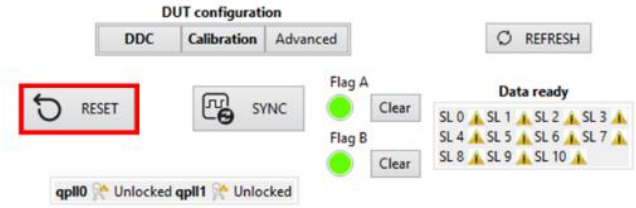
The recommended option to synchronize the HSSL is to click on the “Init sequence” button. It will perform consecutively the below steps (i.e., reset, sync clock and sync) :



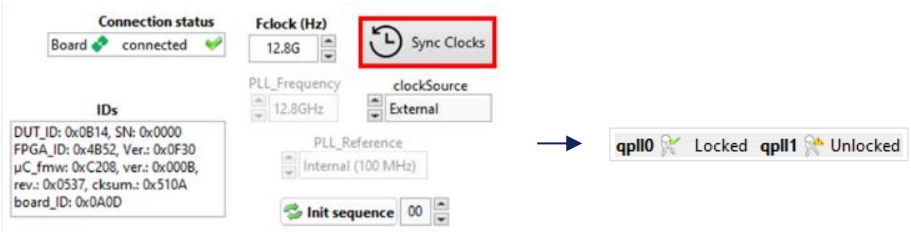
In addition, it will also set the ADC to its optimal settings i.e., TDA = 2 (see section 11) and activate the Background calibration.

The other option is to all steps separately :

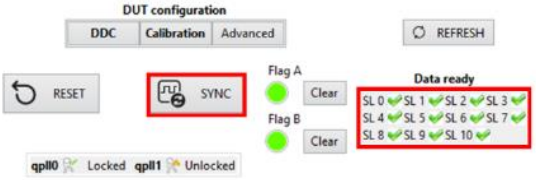
- First click on “Reset” to set the DUT in its default configuration :



- Click on “Sync Clock” to clock the FPGA transceivers with the ADC SSO frequency (slow clock synchronous with the master clock). If successful, the qpll0 or qpll1 indicators should turn to the “Locked” state :



- Click on “Sync” to launch the ESIStream synchronization protocol. The “Data ready” indicators turn green to validate a correct synchronization of each HSSL, seen by the FPGA :



The Flags A and B LED turn red if the SYNC signal distributed internally is too close to a master clock edge. (If a LED is red, it is not an issue for a single device but may be problematic for multi devices synchronization and both LED must be green in this case).

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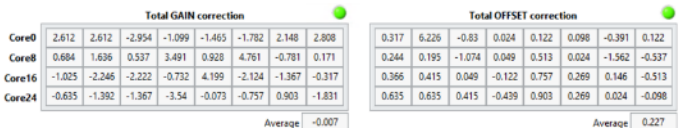
6 Calibration

To modify the calibration settings, click on the “calibration” icon on the DUT control window:

On this window, it is possible:

- To enable/disable Local Factory, Global Factory and Background calibrations,
- To modify the local and global coefficients values
- To modify the value of µ coefficient.

µ is used for the Background calibration and corresponds to the gain and offset step of the algorithm. It is recommended to set it to x00 (corresponding to the fastest calibration convergence). Please refer to the datasheet for additional information about the different calibrations.
If you activate the calibration, click on “Refresh” to see the total correction values:



The total values should not be too close from their limits (± 6.25).
(Note: the "Init sequence" button mentioned previously activates the Background calibration but does not refresh the calibration choice view showing which type of calibration is active)

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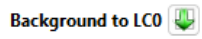
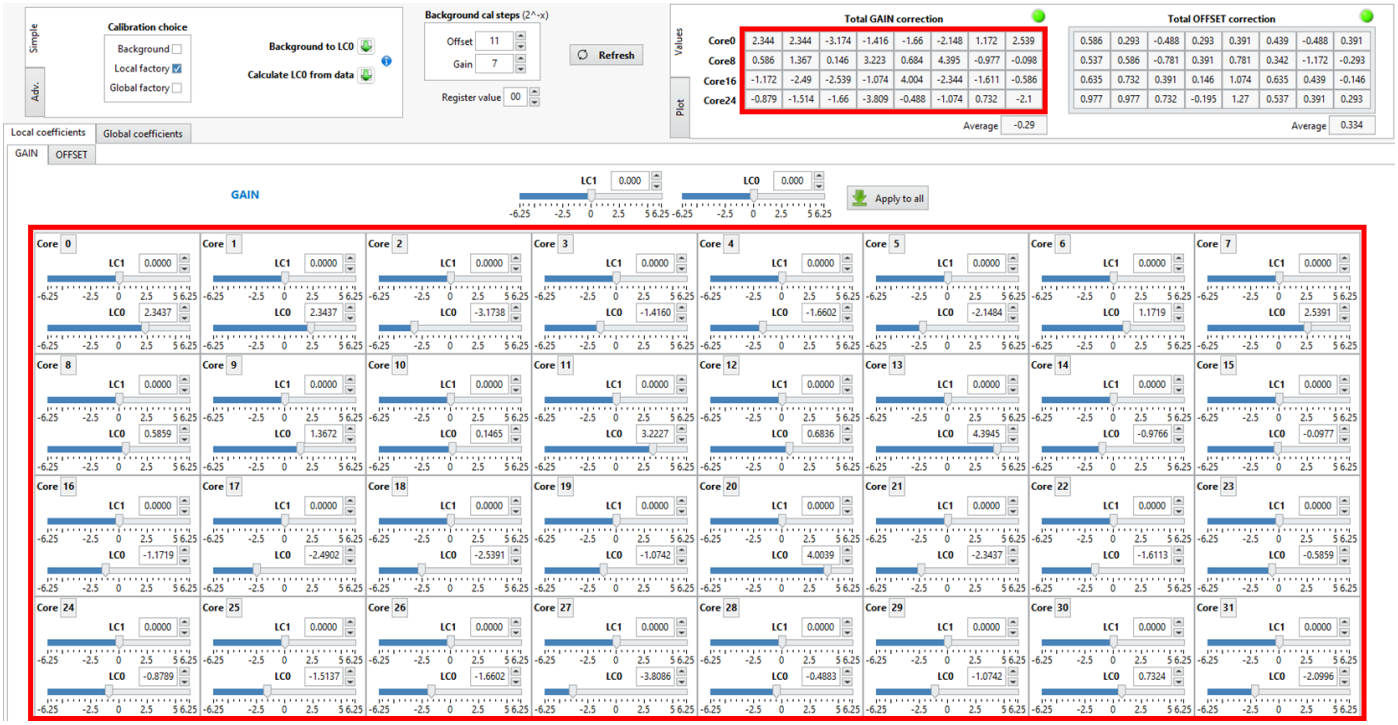
To use the Local Factory calibration with coefficients from the Background calibration, click on the “Background to LC0” button :



This button put the background coefficients of a core in the LC0 (Local Coefficient 0) of the same core (in the picture below, it is shown for the gain but it also applies to the offset) :



Slight differences can happen between the values due to rounding effect.

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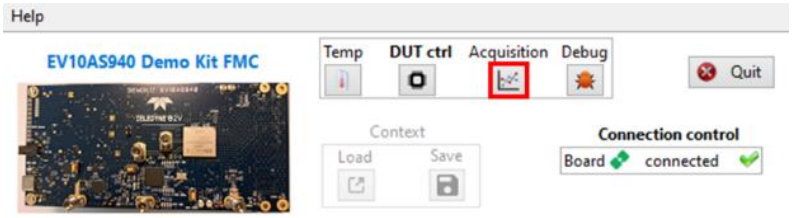
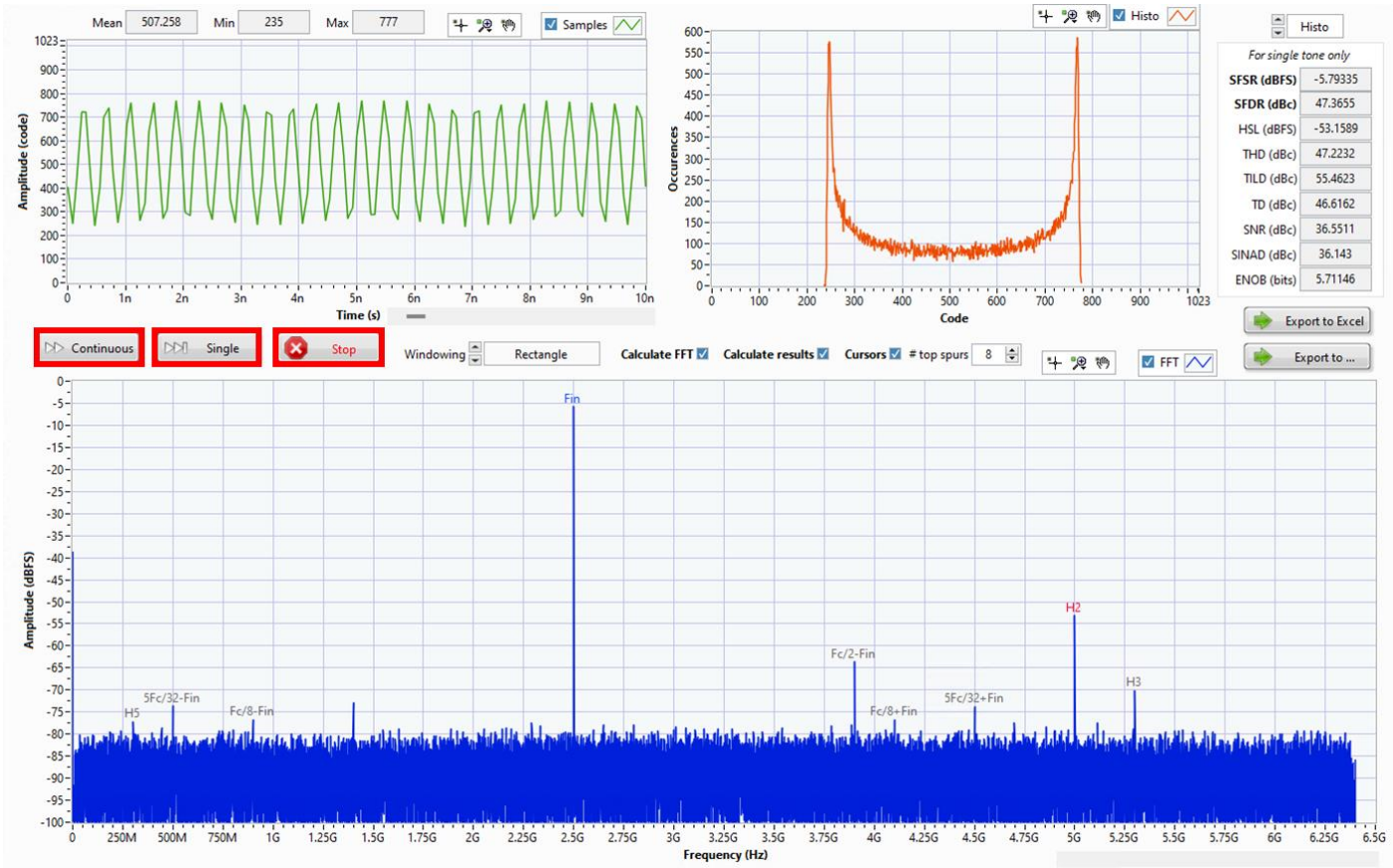
7 Real mode acquisition

7.1 Launch an acquisition

To acquire the data in real mode and calculate its associated performances, click on the “acquisition” button on the main screen :



Click on “Continuous” (perform acquisitions until you click again on the button) or “Single” (one acquisition only) buttons in order to see the samples (top left), the histogram (top right) and the spectrum (bottom) (if you choose continuous acquisition, click on “Stop” or click again on “Continuous”). The acquisition depends on the Nsamples chosen in the DUT control screen :



If the input Fin is not coherent, you can use the “Windowing” control to apply a window to the FFT (no windowing by default):

At the top-right, you can select the curve you want to display between Histogram (chosen by default), INL or DNL :

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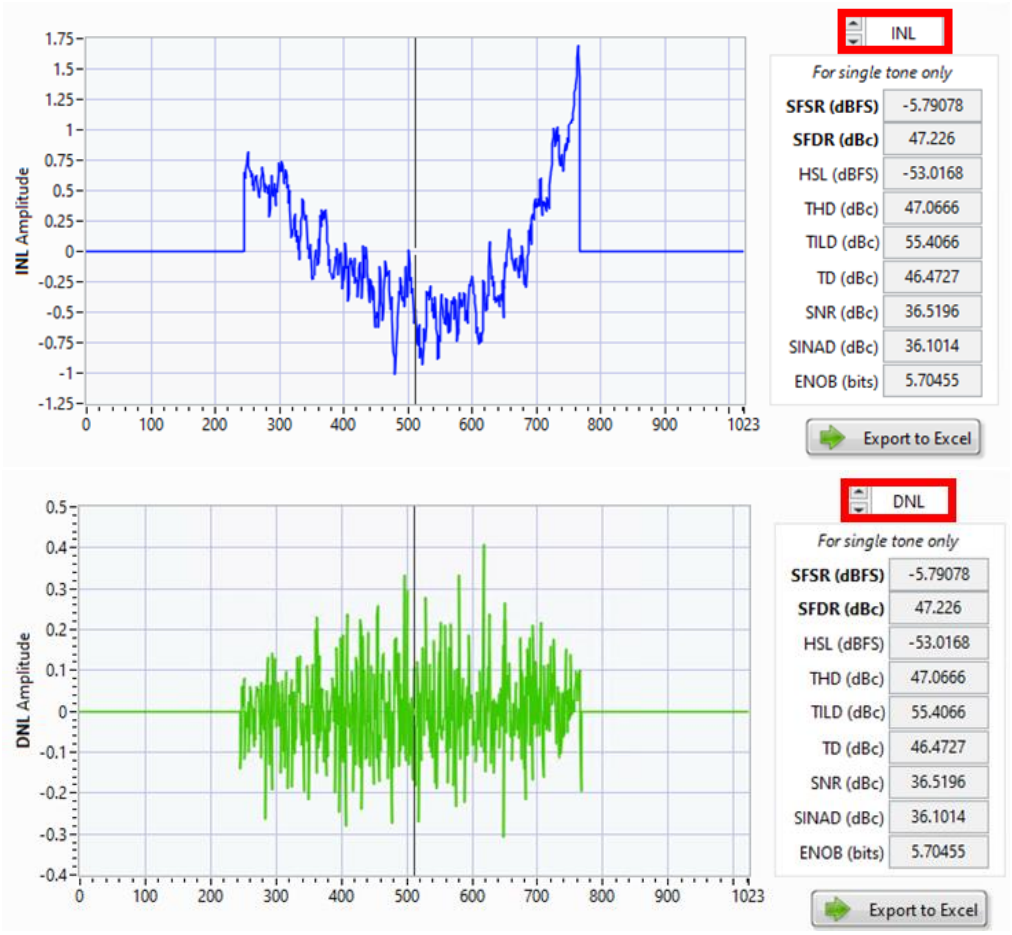
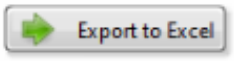


7.2 Export data

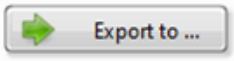
Click on the “Export to Excel” button to export data in an Excel file :



Three sheets are created:

- Samples (which contains the time in ns and the codes of the acquired data)
- Performances (which contains data of the spectrum : SFDR, SNR, …)
- Setup (which contains Fin and Fclk chosen in GHz, the number of samples chosen and the date where the measurement has been done)

If you prefer, you can export data in other formats by clicking on the “Export to …” button :



Clicking on this button will open your repositories for saving the file. Put the format you want in the name of the file (for example, name the file “data.txt” for a text file, or “data.csv” for a csv file).

7.3 Performances

Below are described the calculated performances definitions:

- **SFSR** (Signal Full Scale Range) (dBFS) : Power of the fundamental (highest FFT bin)
- **HSL** (Highest Spur Level) (dBFS) : full scale power of the highest spur (second highest FFT bin, with the condition of having a coherent frequency together with a moderate jitter and number of samples combination so that the Fin occupies a single FFT bin)
- **THD** (Total Harmonic Distortion) (dBc) : power of the 10 first harmonics

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- **TILD** (Total InterLeaving Distortion) (dBc) : power of the interleaving spurs, appearing from the individual core gain and offset mismatches. The spurs are located at Fc/n +-Fin frequencies, n being a power of 2 (up to 32)
- **TD** (Total Distortion) (dBc) : power of all the distortion, harmonics + interleaving: TD = THD + TILD
- **SNR** (Signal to Noise Ratio) : power of the noise (power of all the spurs on the spectrum once the harmonics and interleaving spurs are removed)
- **SINAD** (SIgnal to Noise And Distortion ratio) (dBc) : power of the noise and the distortion: SINAD = SNR + TD
- **ENOB** (Effective Number Of Bits) (dBc) : computed from the SINAD to express an equivalent resolution in bits: ENOB = (SINAD -1.76)/6.02

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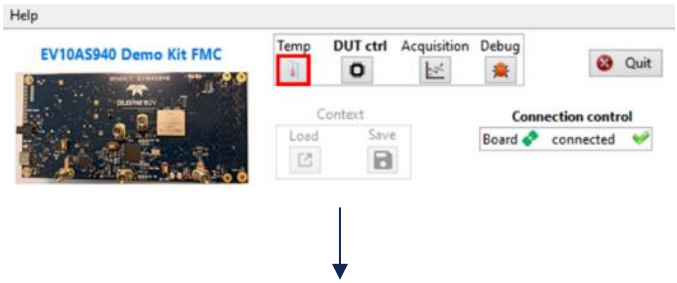
8 Temperature monitoring

To monitor the temperature measured by the diode and by the internal sensor, click on the “Temp” button in the main screen:



The temperatures measured by the diode and by the internal sensor are displayed (if the “Enable” checkbox is ticked for the sensor). It is recommended to set the averaging of the internal sensor to 16 to smooth the curve.

The internal sensor uses a coefficient to compute the temperature, written in a dedicated register. This coefficient default value is set to 0xCCE4 in the GUI (determined from an averaging on several parts) and may then be optimized with the part in use on the current board to better match the diode temperature.

Additionally, the “Refresh Rate (s)” at 5 seconds by default can be modified if necessary and it is possible to choose the curves to display by clicking on the corresponding checkbox.

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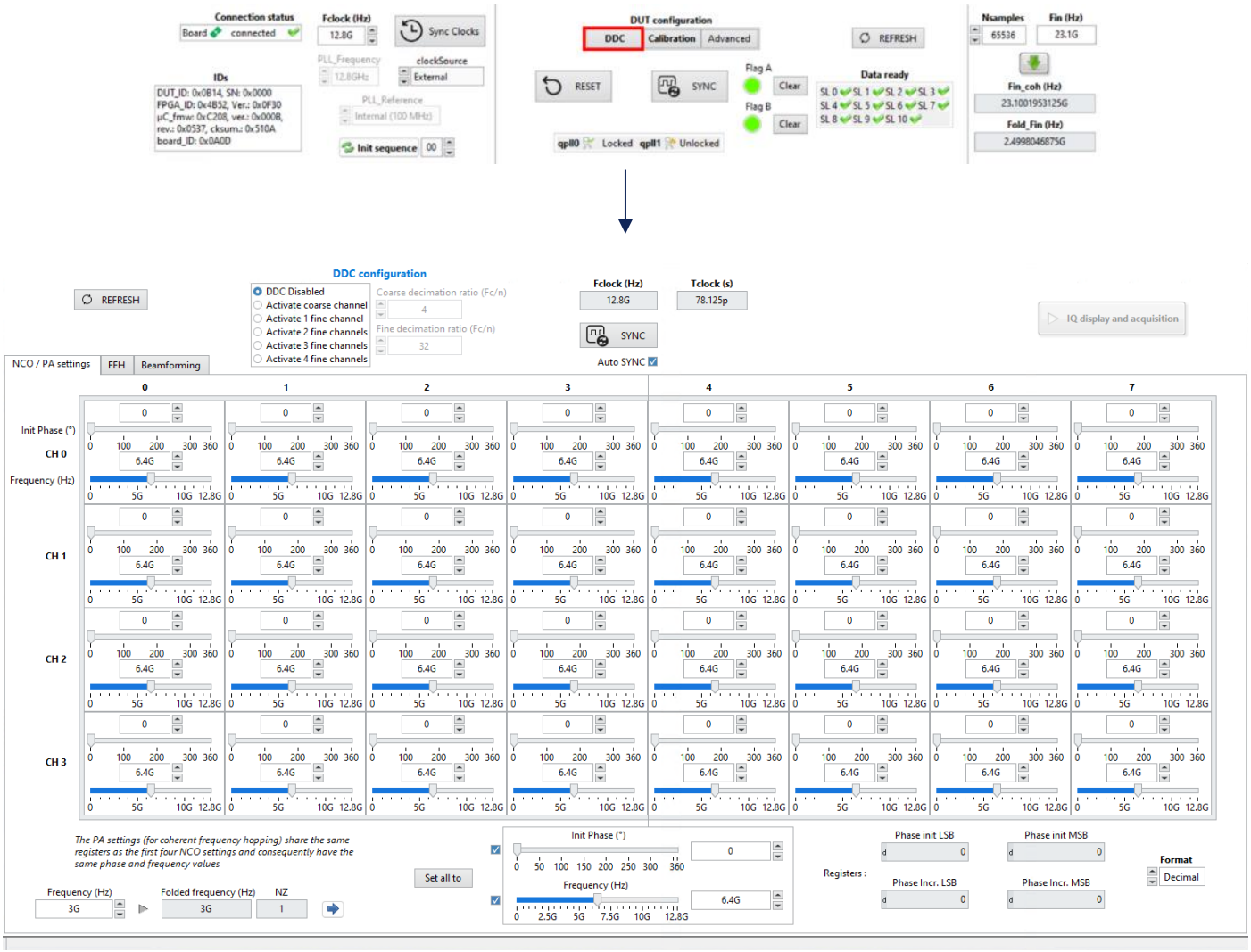
9 Complex mode configuration

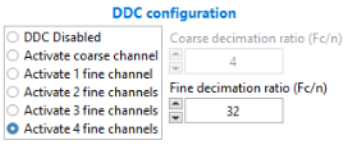
To configure and use the digital features, click on the DDC button on the DUT control window:



9.1 DDC configuration

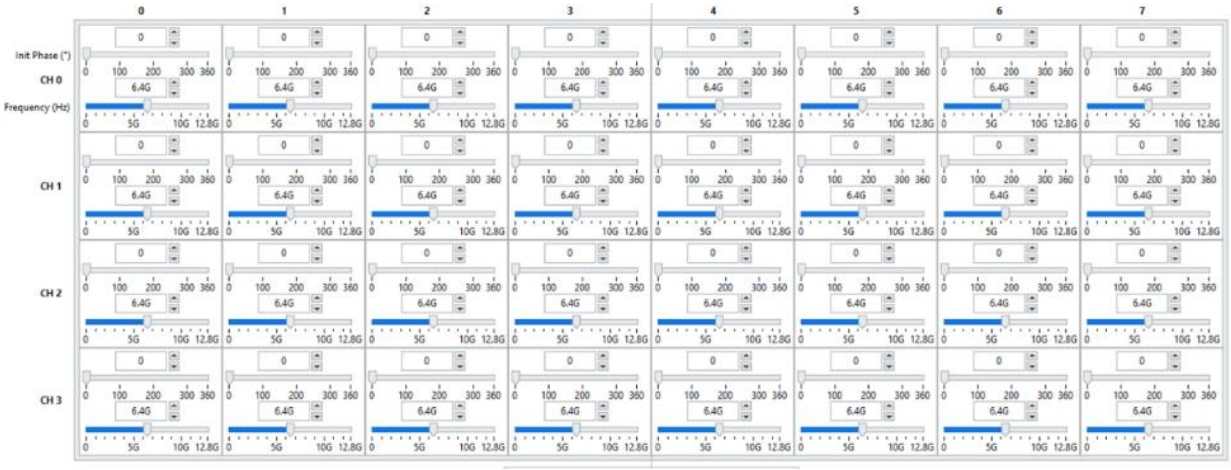
On the top part of the window, the DDC configuration section allows setting the ADC in its various complex modes:

- Type and number of channels (1 coarse or from 1 to 4 fine)
- Decimation ratio (from 4 to 32 in coarse, 32 to 2048 in fine)

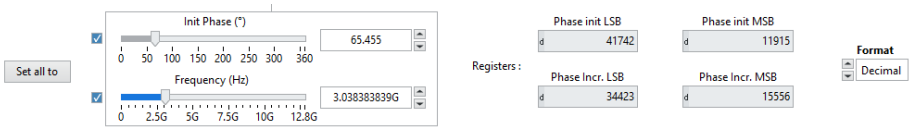


9.2 NCO/PA settings

On the NCO/PA settings tab are represented all the possible NCO settings. Since the fast frequency hopping can use up to 8 settings for the 4 channels, 32 initial phase and frequency values can be configured:



In the bottom part, a control can be used to set all the settings to a specific value (for the phase and/or the frequency). At its right are displayed the corresponding raw values that will be written to the registers (2 registers, LSB and MSB, used for both the phase and frequency):



As mentioned in the bottom left part, if the frequency hopping is set to the coherent hop mode, it will rely on four phase accumulators that use the first four NCO settings.

9.3 Fast Frequency Hoping

Below is shown the Fast Frequency Hoping (FFH) tab content:

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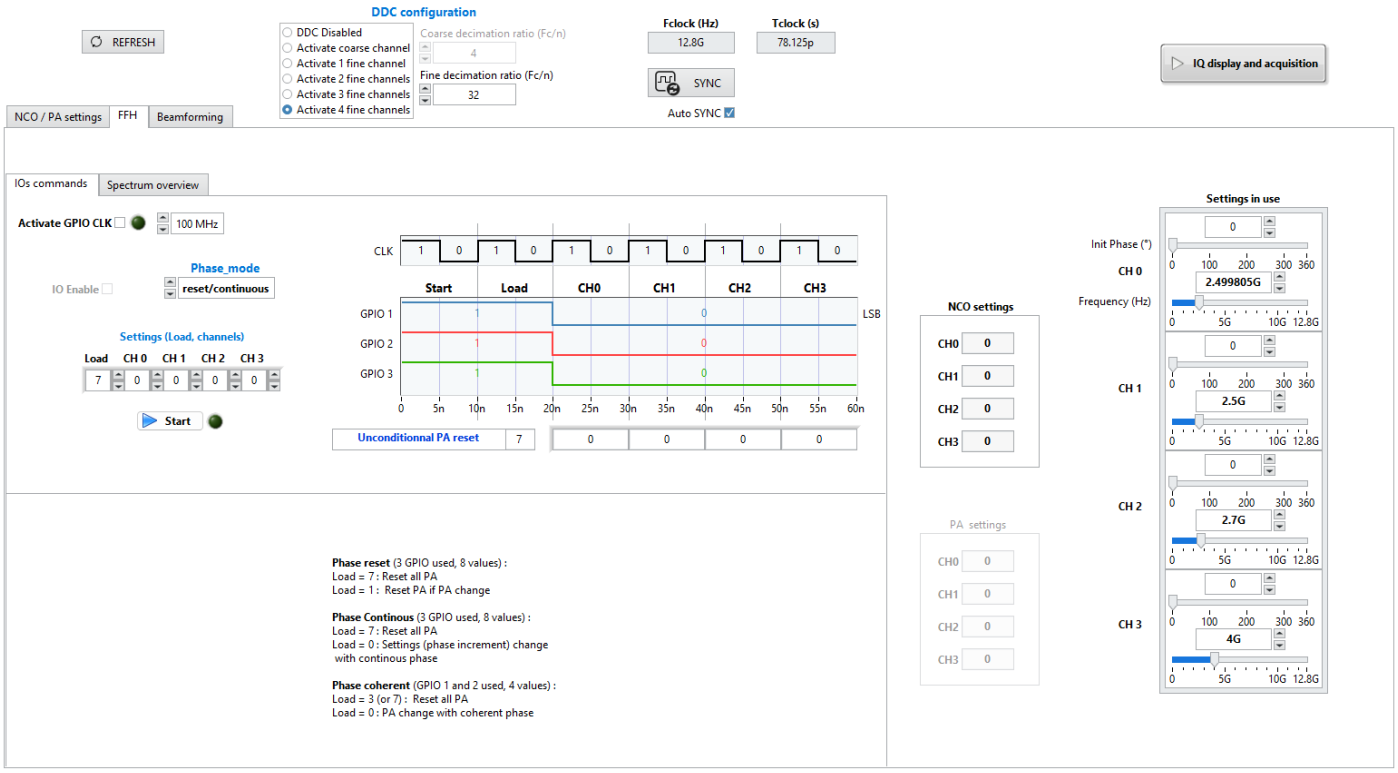
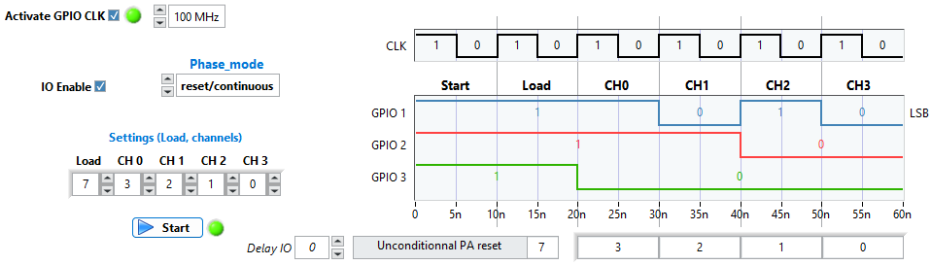


9.3.1 IOs commands

To use the FFH, it is first required to activate the GPIO clock (either at 50 or 100 MHz). A LED turns green to validate that the clock has been successfully received by the FPGA.
Then, the IO enable control can be activated and the phase mode can be set to “reset/continuous” or “coherent”:

The diagram on the right illustrates the signals that are sent on the GPIOs depending on the kind of hop (Load) and the NCO/PA settings zone desired for each channel. The example below shows a RTZ hop with channel 0 using settings 3, channel 1 using settings 2, channel 2 using settings 1 and channel 3 using settings 0:



Pressing the button “start” will trigger the FPGA to send the GPIOs signals to the dedicated ADC pins. The LED beside will turn green to validate a correct hop (it checks if the status registers indicating the zones in use per channel correspond to the required ones).

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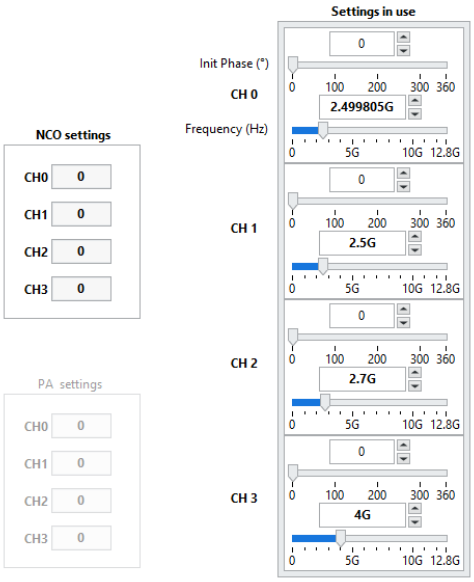
9.3.2 NCO/PA Settings in use

On the right are displayed the settings index and phase/frequency values currently in use for each channel, NCO settings in case of reset/continuous hops, PA settings for coherent hops.



The settings can be modified directly on the control and the full list on the NCO/PA settings tab will then be updated.

9.3.3 Spectrum overview

The spectrum overview tab pictures the channel settings in use on the Nyquist zone by displaying their position and width from their NCO frequency and decimation factor.

In addition, clicking on the “Update real spectrum” button will trigger an acquisition in real mode to precisely know which frequency content will be acquired relatively to the channels settings (the complex mode previously in use is programmed again after the real mode acquisition). The number of points to be acquired can be changed depending on the requirements in term of noise floor level. It is preferable to not exceed 64k points to avoid slow down due to the high number of points display.

It is also possible to directly change the channel position by grabbing the channel center dotted line and moving it on another frequency in the Nyquist zone. The “settings in use” frequencies will then be updated accordingly.
The next plot shows the results of an acquisition, using an input frequency at 2.5 GHz with the DDC configuration set to four channels with a 64 decimation ratio and different NCO frequency settings :

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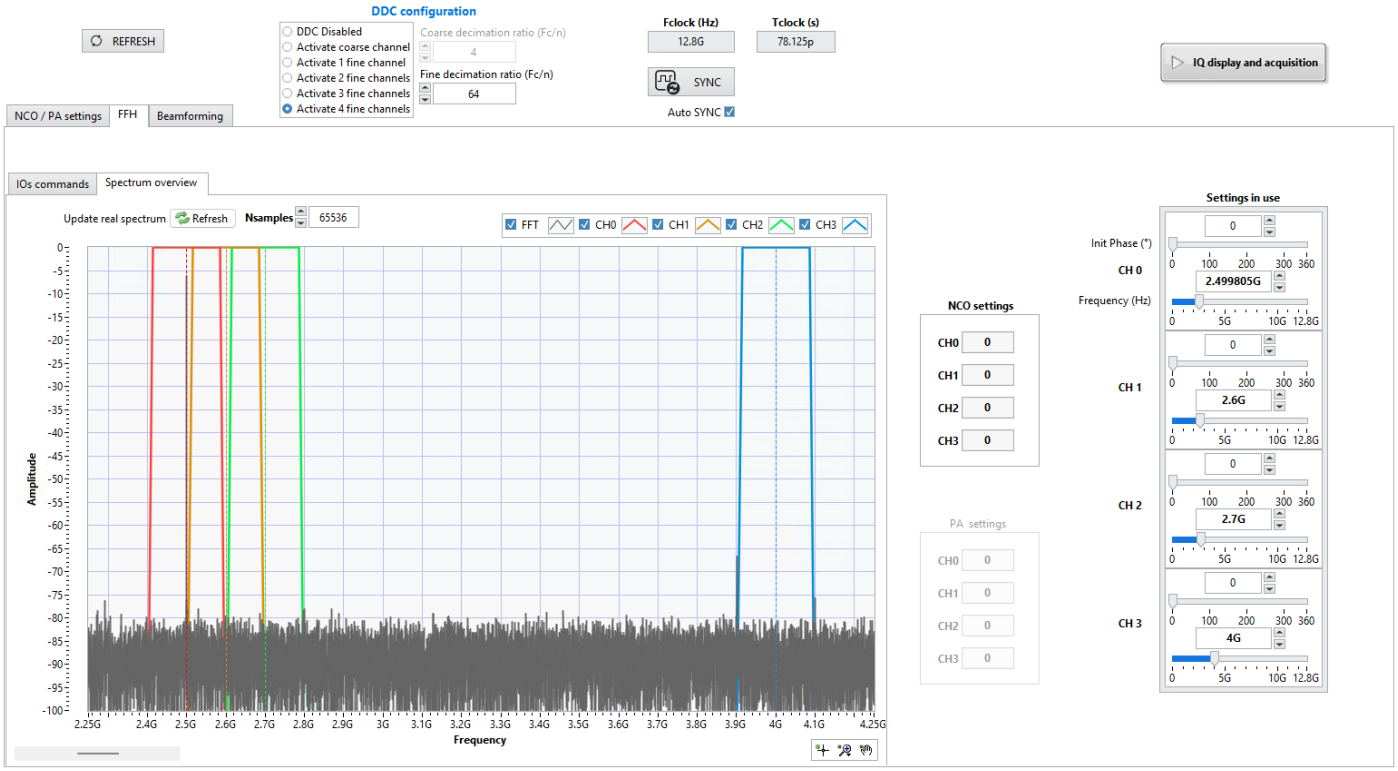
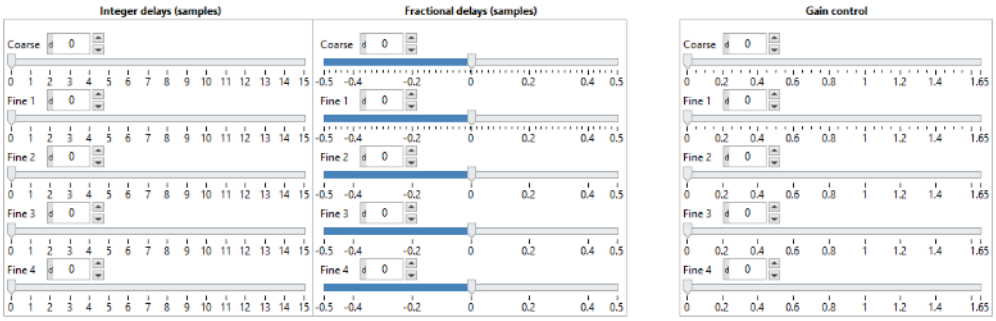


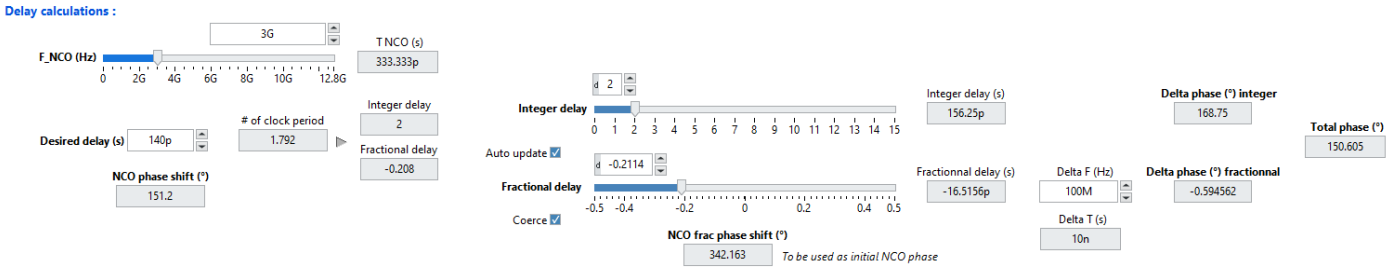
9.4 Beamforming

The beamforming tab gives access to the corresponding delay and gain settings :



The gain varies from 0 to 1.65 and there are two kinds of delays: the integer delays will add from 0 to 15 Tclock to a channel while the fractional delay is based on a farrow filter to add from -0.5 to 0.5 Tclock.

At the bottom part are displayed several calculations that can be useful for a proper delays configuration. Below is an example for Fclock=12.8 GHz, a NCO frequency at 3 GHz and a desired delay of 140 ps :



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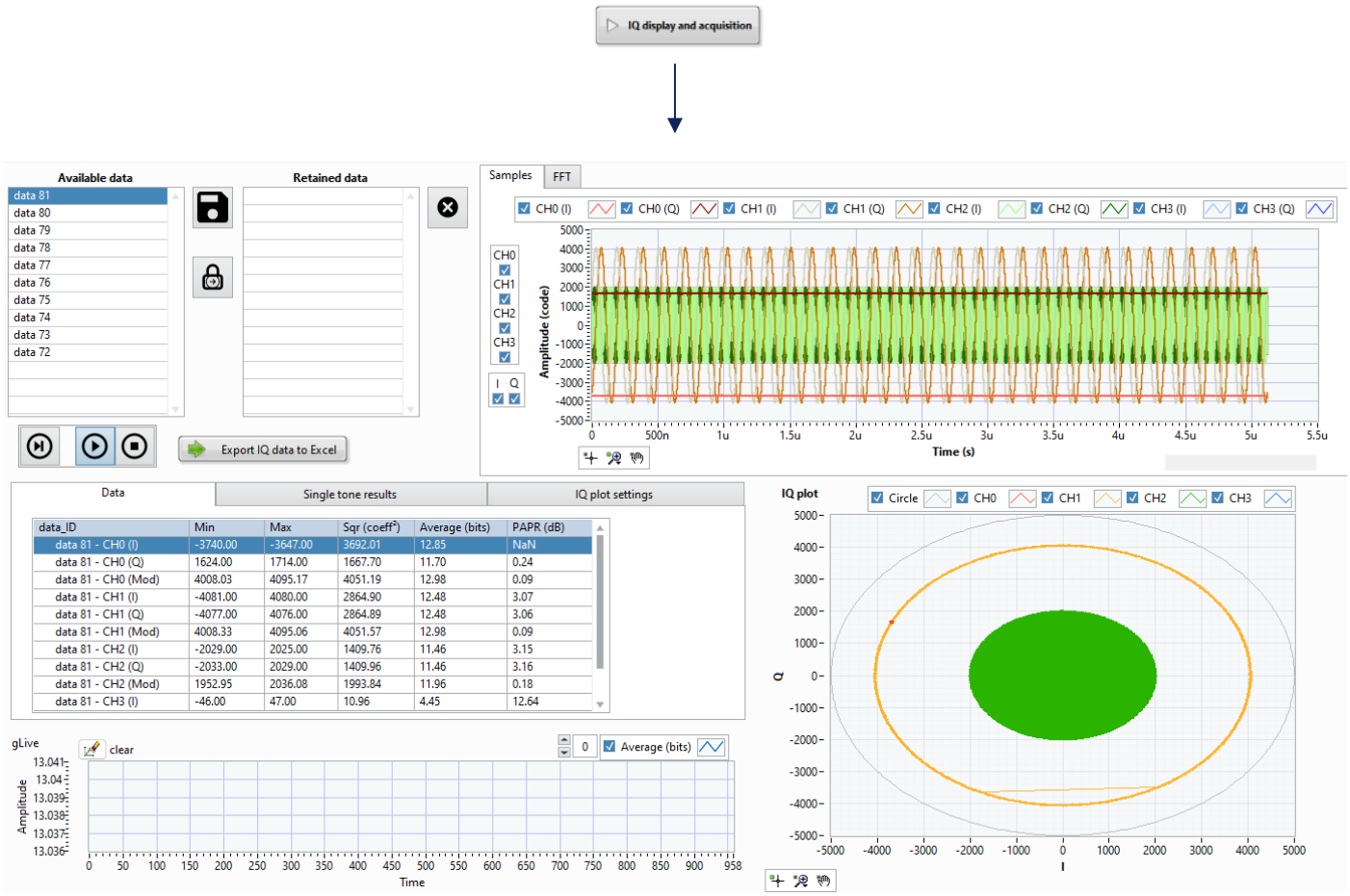
The 140 ps delay corresponds to 1.792 clock period which can be expressed into 2 integer delays and -0.208 fractional delay.
Consequently, those values must be set to the corresponding controls. In addition, the NCO initial phase has to be shifted to account for the fractional delay. In this example, the phase shift to be applied is equal to 342,163° as displayed in the bottom part.

9.5 IQ display and acquisition

To display and acquire IQ data in complex modes, click on “IQ display and acquisition” button:



The acquisition can be performed in single (left) or continuous (middle) mode. The button stop (right) is used to stop a continuous acquisition:

In the bottom right are displayed the IQ data for each channel in the form of a IQ plot. On the top right, on the tab “sample”, the IQ are plotted as waveforms (for each I, Q and channels).
On the tab “FFT” are represented the spectra of each channel.

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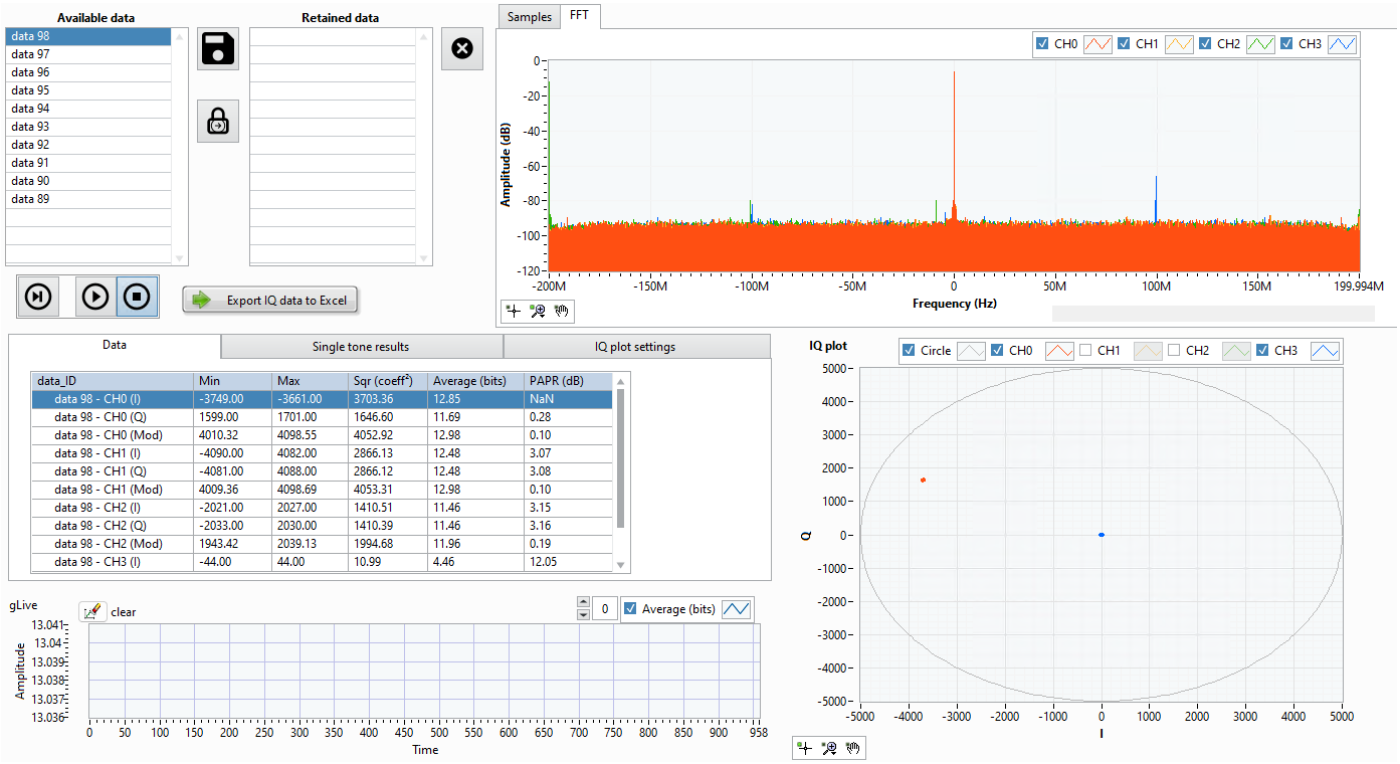

It is also possible to export the IQ data of all channels by pressing the “Export IQ data to Excel” button :

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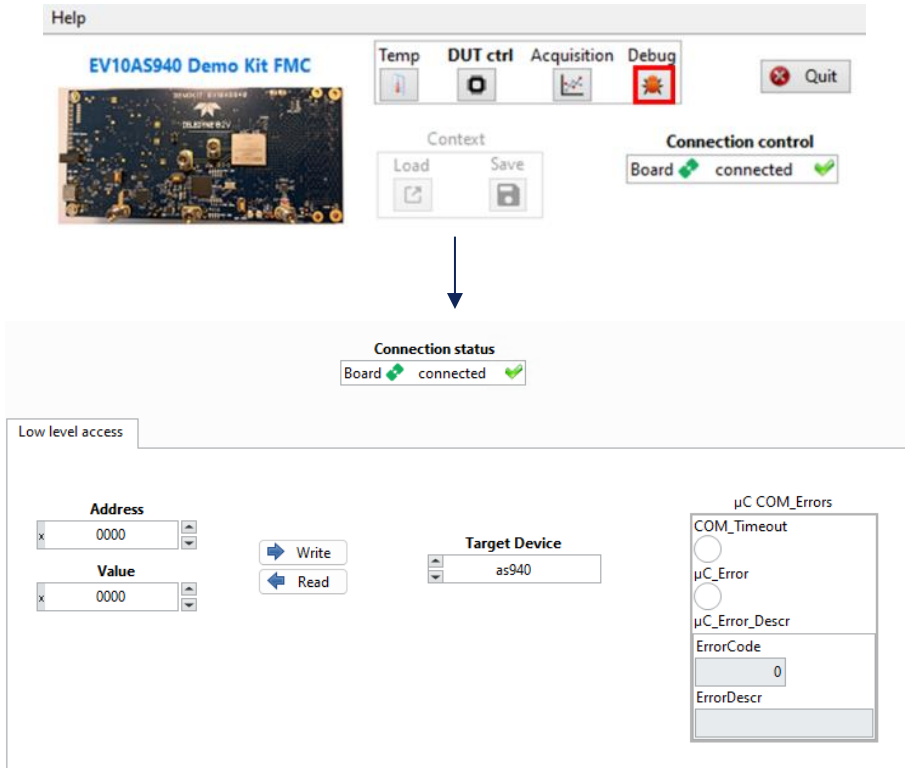
10 Debug window

To read/write values in the different registers, click on the “Debug” icon in the main screen:



First, select the device and enter the address of the register in hexadecimal format :

- If you want to read a register, click on the “Read” button and look at the value in the “Value” control.
- If you want to write a value in a register, enter the value in the “Value” control and then click on the “Write” button.

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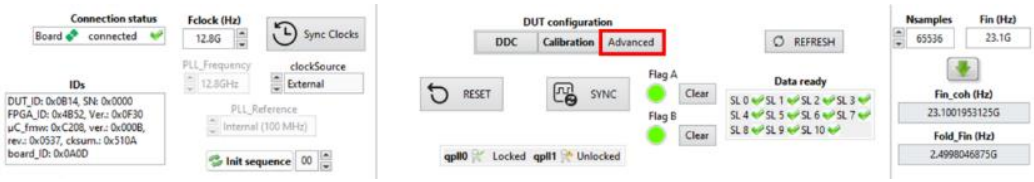
11 Advanced settings

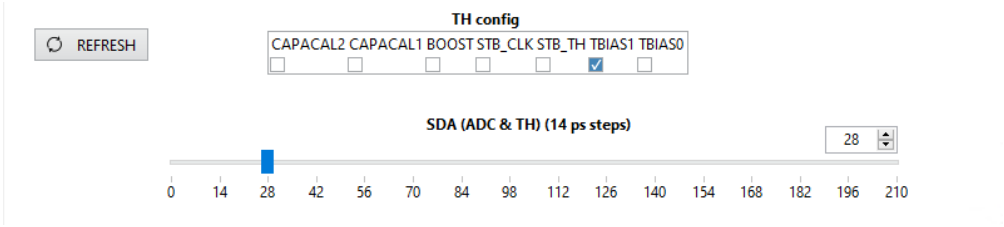
Click on the “Advanced” button:



Here you can modify the parameters of the TH and the SDA:

- CAPACAL 1, CAPACAL 2 and BOOST: to improve performances like SFDR at high Fin, especially above 20-25 GHz
- STB_CLK, STB_TH: standby mode, to be left untouched.
- TBIAS1 and TBIAS0: internal biasing, to be left untouched.
- SDA (or TDA): Timer Delay Adjust, register 0x1076, optimal value found to be 2 (6 by default)

If you have modified the SDA (for example if you did the Init sequence), click on “Refresh” to update the display of the parameters:



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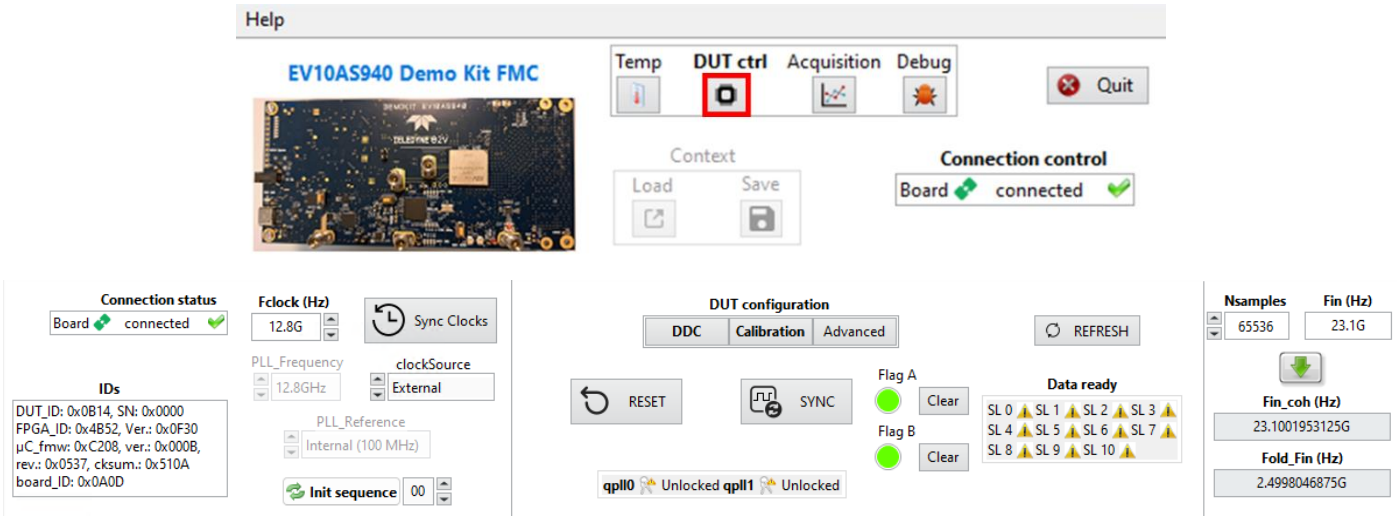
12 Quick startup

Here is a summary of the steps required to quicky perform an acquisition in real mode with the ADC configured in its optimal settings:

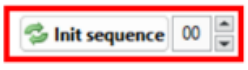
- **Connect the board :**

- **Open the DUT control window :**

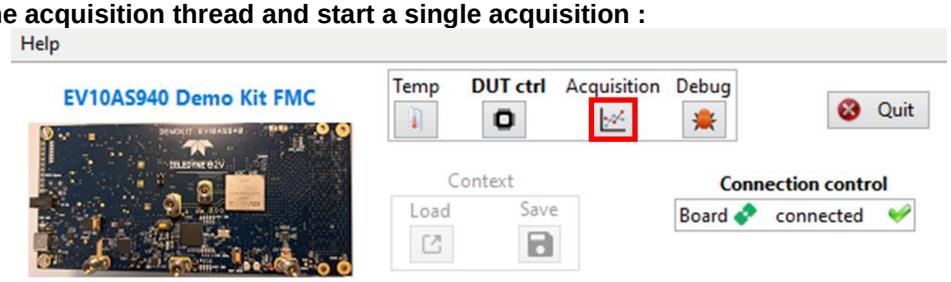


- **Configure the clock source (external or internal) and its frequency :**

- **Start the initialization sequence :**



- **Open the acquisition thread and start a single acquisition :**



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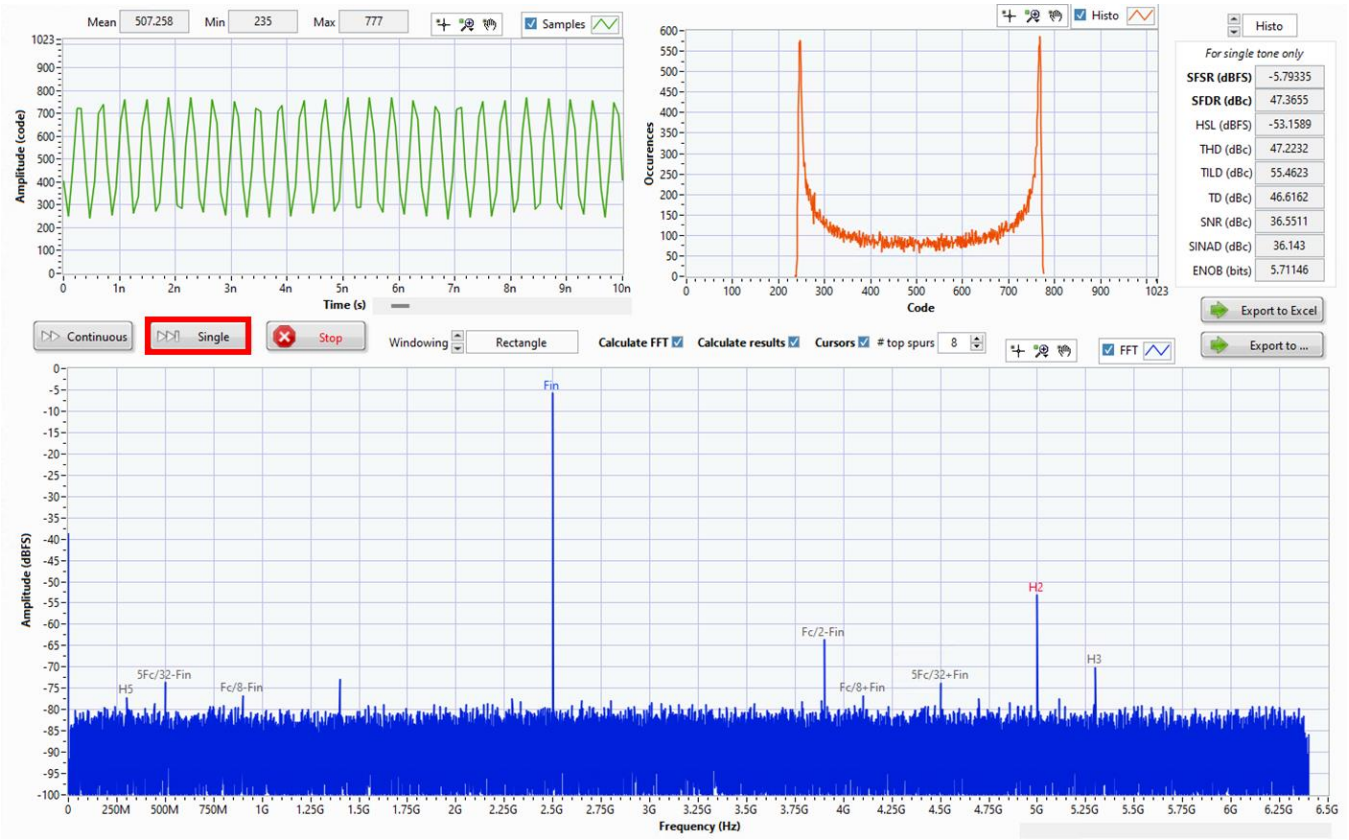

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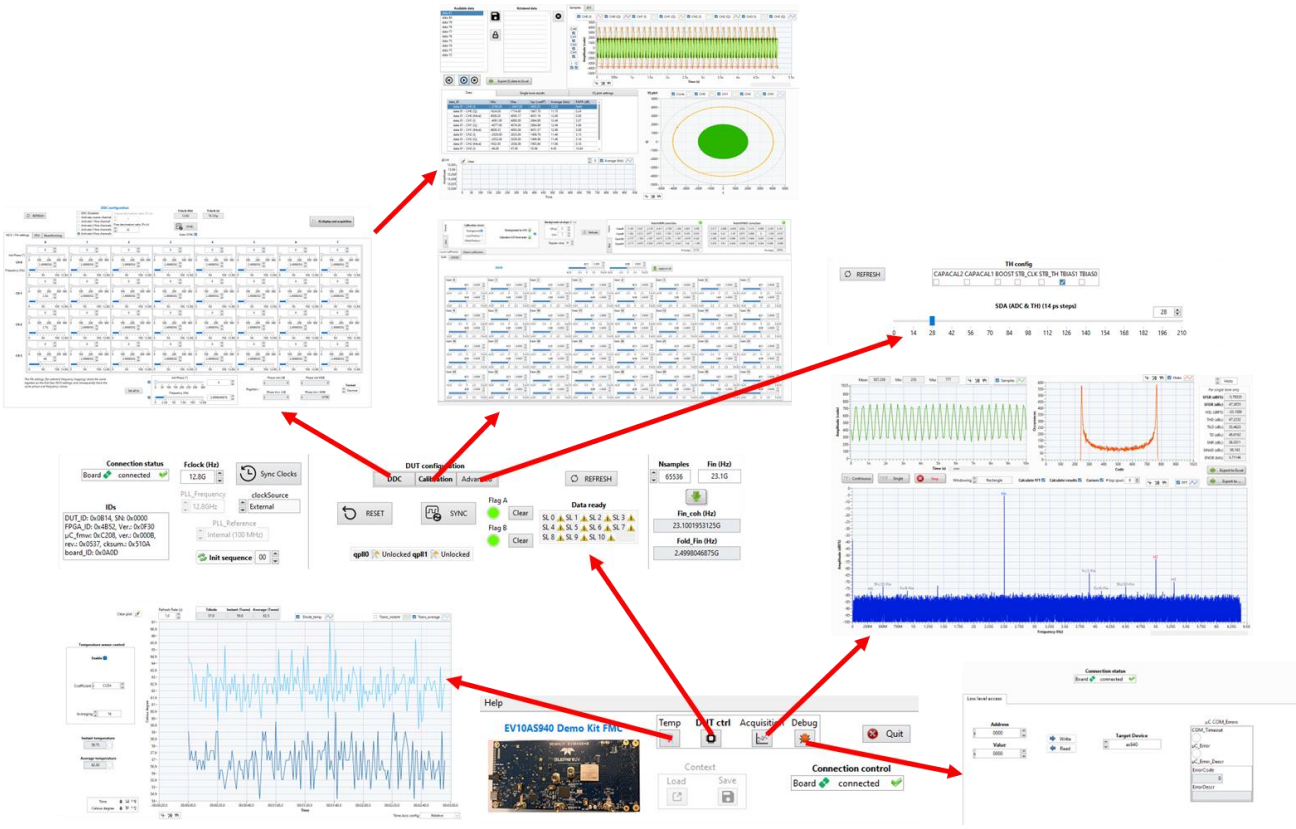
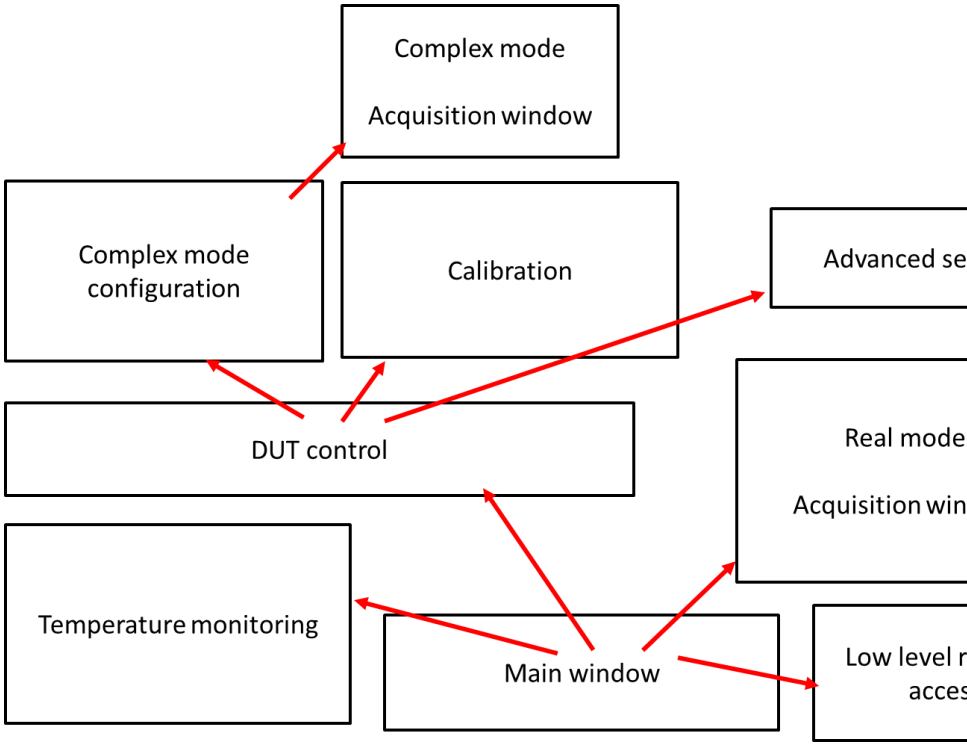
13 Windows overview

Here is an overview of the different windows of the GUI with their description below:





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14 Troubleshooting

- Connection with the board not possible:
  - Check the USB connection
  - Press the µC reset button on the board
  - Restart the GUI or disconnect/reconnect the board by clicking on the board icon in the main GUI window

- Curve of the internal temperature sensor stay at a fixed value :
  - Check that the clock source is wired

- HSSL synchronization not possible:
  - If serial links are not connected or both QPLL are not locked, check if frequency clock on your generators are the same as those put in the GUI
  - If Flag A and/or Flag B are red, press SYNC again until Flag A and Flag B are green.

- Spectrum with degraded performances:
  - Restart the init sequence and check the total calibration coefficients. applied (sometimes when conditions change (for example if Fin change) the calibration saturates, so in this case it is necessary to disable and enable again the background calibration)
  - Check Fin ≠ n*Fclk/64 (Fin ≠ n*200 MHz for Fclk = 12.8 GHz) when Background calibration is enabled, or switch to the Local Factory calibration thanks to the “Background to local” button

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